UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF NEW YORK

ADVANCED VIDEO TECHNOLOGIES LLC, Plaintiff, v. HTC CORPORATION and HTC AMERICA, INC., Defendants.	: : : : : : : x	**ECF CASE** Civil Action No. 1:11-cv-6604-CM-RLE District Judge Colleen McMahon Magistrate Judge Ronald L. Ellis
ADVANCED VIDEO TECHNOLOGIES LLC, Plaintiff, v. RESEARCH IN MOTION, LTD. and RESEARCH IN MOTION CORPORATION, Defendants.	: : : : : : : : x	**ECF CASE** Civil Action No. 1:11-cv-8908-CM-RLE District Judge Colleen McMahon Magistrate Judge Ronald L. Ellis
ADVANCED VIDEO TECHNOLOGIES LLC, Plaintiff, v. MOTOROLA MOBILITY, LLC., Defendant.	: : : : : : : x	**ECF CASE** Civil Action No. 1:12-cv-918-CM District Judge Colleen McMahon Magistrate Judge Ronald L. Ellis

DECLARATION OF DR. PAUL D. FRANZON IN
OPPOSITION TO DEFENDANTS' MOTION FOR SUMMARY JUDGMENT
OF INVALIDITY BASED UPON ALLEGED LACK OF WRITTEN DESCRIPTION

I, Paul D. Franzon, do declare and state as follows:

1. I submit this declaration in opposition to Defendants' Motion For Summary Judgment of invalidity of U.S. Patent 5,781,788 entitled "Full Duplex Single Chip Video Codec" ("the '788 patent").

2. I am presently an Alumni Distinguished Professor of Electrical and Computer Engineering at North Carolina State University in Raleigh, North Carolina.

3. My employment history, education, professional activities, patents, and other miscellaneous publications are set forth in my CV, attached as Exhibit 1.

4. I have over 25 years experience in the design and development of electronics and software systems. I have considerable experience in the fields of digital signal processing, including sonar, radar and video. I also have extensive experience in design and development of integrated circuits and systems, including digital signal processors, networking, computing/graphics processors and video codecs.

5. I received a Bachelor of Science in Physics and Mathematics from the University of Adelaide, Australia, in 1983. While I was an undergraduate, I designed a CCD video camera with a digital interface as an intern at DSTO Australia. I also received a Bachelor of Engineering with first class honours in Electrical and Electronics Engineering from Adelaide University in 1984. In 1989 I received a Ph.D. in Electrical and Electronic Engineering from Adelaide University. My Ph.D. thesis was entitled "Fault Tolerance in VLSI" and involved investigating schemes to make very large digital signal processing chips that could withstand inevitable manufacturing defects.

6. During the course of obtaining my Ph.D., I worked as a consultant at AT&T Bell Laboratories in Holmdel, New Jersey during 1986 and 1987. My work as a consultant with Bell Laboratories involved designing and building the VLSI chips that were the focus of my doctoral dissertation.

7. Since 1989, I have been a Professor of Electrical and Computer Engineering at North Carolina State. During that time my focus has been on chip and system design. I have led numerous research projects in this area including the design and building of numerous digital and mixed signal chips. In addition, I have taught classes in digital chip design and interfacing. Past

examples of projects include components of video codecs, DSP processors, computing, graphic systems, speech recognition, network security, packet processing and wireless communications. Video codec projects have included the design of different motion estimators.

8. Since 1989 I have also been almost continuously working in industry in one way or another. These include consulting for MCNC; Techsearch International; Data Communications Technologies, Inc. ("DCT"); Cadence Design Systems, Inc.; Mentor Graphics, Inc.; Polychip; Ericsson, Inc.; Sofrent; CAPPS; Venture 2000; LightSpin Technologies, Inc.; Talon Logic Corp.; Irvine Sensors Corp.; Tessera Inc.; Rambus Inc; and DARPA.

9. In 1995-1996, I consulted for DCT, a spinout from RTI International. There I was involved in the architecture and design of H.262 and H.263 video codecs. These standards employ much the same encoding and decoding algorithms as used in H.261, which is the first member of the H.26x family of standards. In this engagement, I designed the memory interface for an H.263 video codec and was involved in architecting an H.262 encoder. My responsibilities included generating engineering drawings and writing and verifying Verilog hardware description code.

10. Between 1994 and 2000, I consulted to Polychip on the circuit design of chip to chip and chip to memory interfaces. In 2000 – 2002, I was Vice President of Engineering for LightSpin, a company I co-founded. LightSpin developed photonic chip-to-chip interfaces. As Vice President of Engineering my responsibilities included leading a team the fabricated and tested novel photonic devices and I worked personally on circuit design issues.

11. In 2005 to 2006, at Talon Logic and Irvine Sensors, I was involved in architecting security chips. In these engagements, I was involved in architecting the solution, which included preparing engineering drawings. At Irvine, the project focused on intrusion detection in

computer networks.

12. From 2009 to 2012, I held a part time position with Rambus as a technical director. As technical director, my main focus was working on cost effective solutions to building stackable dynamic random access memory (DRAM) chips. As part of this effort, I wrote the Verilog hardware description code that described the repair and yield portion of the memory controller for the DRAM stack. I led a team that worked out solution at the bank and sub-bank level for test and repair of high capacity 3-dimensional DRAM systems. During this time I also served as technical advisor to Tessera on 3DIC related issues.

13. I have co-authored three books and over 200 journal and conference publications, primarily in the areas related to chip design. One chapter in the book Smith and Franzon, "Verilog Styles for Synthesis of Digital Systems" includes the detailed design of a motion estimator as would be used in H.26x codecs. Many of my publications have dealt with interfacing digital signal processors, network processing chips and speech recognition chips with memory subsystems incorporating DRAMs, i.e., dynamic random access memories. Often this work included the optimization of system performance and cost by employing the proper mix of memories.

14. I have also won the Alcoa Research Award and the New South Wales Ex-Patriot Scientist Award for my work in chip design. I have also been elevated to the rank of Fellow of the Institute of Electrical and Electronic Engineering, to which only 0.1% of members can be selected in a given year.

15. I am one of the inventors on five issued U.S. Patents including 8,208,578; 6,985,483; 6,934,252; 6,927,490; and 6,885,090. I am also an inventor on the following four published U.S. applications: 20130069709; 20120175696; 20110310992; 20070297216; and

20070128744. I also have an additional eight unpublished applications currently pending before the U.S. PTO.

16. For my engagement with AVT, I am being compensated at a rate of $300/hr, which includes my time for preparing this report. My compensation is not dependent on the outcome of this case.

17. In my opinion, one of ordinary skill in the art, with respect to the '788 Patent as of May 8, 1995, would have at least a master's degree in electrical engineering, or a bachelor's degree with equivalent work experience, and, in addition, at least three years' experience in digital signal processing, including the design and development of chip sets and systems that do image and/or video processing. I personally worked with such people at the time and became familiar with their skill sets.

18. I have been advised that the legal standard for written description requires an objective inquiry into the four corners of the '788 patent from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to one skilled in the art and show that the inventor actually invented the invention claimed as of the filing date of patent. The specification does not need to provide support using exactly the same terms as the claims at issue. The specification need only reasonably convey to one skilled in the art that the inventor possessed the invention claimed. Further, if a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate written description requirement is met.

19. In my opinion, it would have been clear to a person of ordinary skill in the art as of May 8, 1995, that there is written description support in the '788 patent for "interim storage of

. . . outgoing video data." In addition, there is clear support for this term as interpreted by the Court to mean "temporary storage of video data that has been decompressed prior to its passing through the video output connection to the monitor." Further, the patent provides written description support for the so called "wherein" clause [2], which is "wherein the outgoing video data is decompressed data supplied to the video output connection." It is also my opinion that the term "interim storage of . . . outgoing video data" as described in the '788 Patent is not limited to data that is only ready for output on a NTSC or PAL compatible monitor. In the remainder of this declaration, in each instance in which I refer to what is described in the '788 patent, or what a portion of the '788 patent means to me, it should be understood that I am expressing my professional opinion as to what would have been seen and understood by one of ordinary skill as described above.

20. In arriving at my opinions, I reviewed the '788 patent (Dkt.57-1, *HTC* Action); the Court's Claim Construction Order (Dkt.52, *HTC* Action); Defendants' Joint Memorandum in Support of Motion for Summary Judgment of Invalidity (Dkt.56, *HTC* Action) and exhibits; the original prosecution history of the '788 patent (Dkts.31-5 to 31-19, *HTC* Action); the reexamination prosecution history of the '788 patent (Dkts.31-20 to 31-33, *HTC* Action); and U.S. Patent 5,491,515 to Suzuki, et al. (Exhibit 2) and Bose, et al., article entitled "A Single Chip Multistandard Video Codec" (Exhibit 3), which are prior art relied on by the Examiner during reexamination of the '788 patent.

21. The '788 patent discloses a single chip implementation of a video encoder and decoder that uses an external dynamic random access memory ("DRAM"). ('788 patent, Fig. 1.) Figure 1 describes all the interfaces to the chip 12. Those interfaces include ones for uncompressed video data from a video source 14, decompressed video data to a display monitor

16 and transmit and receive interfaces for compressed video data. In addition, it describes an on-board interface to a DRAM 18 and a system bus 24. As shown in Figure 1, the video codec operates as both an encoder and decoder. In the '788 Patent, the term video codecs is used to refer to "video compression/decompression processors (video codecs)." ('788 patent col. 1, lines 8-13.) The term video codec is also synonymously used to mean a "video <u>co</u>der/<u>dec</u>oder." The term video codec refers to a process that converts video data to and from a fixed format, which in this case includes compression/de-compression within that format.

22. For the encoder, it receives an uncompressed video bit stream from a video source 14, encodes it using a video encoding algorithm and outputs the encoded video bit stream to the transmit channel 20. For the decoder, the chip receives a compressed video bit stream from the receive channel 22, decodes it and outputs a decoded or decompressed video bit stream.

23. The background of the patent indicates that television signals are made of individual frames sequenced one after another. ('788 1:22-25.) Each frame can hold many pixels. A "pixel" is the smallest element of a picture, and often specifically of a digital image. In the patent, the term pixel is used to refer to a picture element. Since approximately 30 frames per minute are used for video, uncompressed video bit streams contain many millions of pixels per second. ('788 1:25-30.) Thus, you need digital compression techniques to reduce the required video channel bandwidth. ('788 1:31-32.)

24. There are closely related set of standards generally referred as H.26X. The first of these was H.261, which is specifically mentioned in the '788 patent. ('788 1:49.) H.261 was followed by the H.262, 263 and 264 standards. The H.261 standard is a recommendation for a video codec. It primarily describes the encoding scheme and formats for the transmitted and compressed data. Given the amount of data generated in capturing a video, for example, the

H.261 standard naturally requires large amounts of memory and fast processing to handle the millions of pixels per second that need to be compressed or decompressed. Although the standards describe an exchange data format they do not describe how to set up all the details in the encoder to get efficient compression.

25. The '788 patent discloses a single chip implementation that permits efficient encoding and decoding of video data.

26. In essence, video encoding uses three techniques (1) motion estimation, (2) discrete cosine transforms (DCT) and (3) variable length coding. Motion estimation uses the fact that often successive frames of video are different only in that objects have moved and thus all you need is the distance and direction of movement to encode a later frame of video data. DCT compresses spatial information in a video frame, for example a blank wall has little spatial variation. Variable length coding recodes frequent and long datums using short code words.

27. For example, in motion estimation two successive frames of video are compared in detail to determine if part of the second frame consists of a reference block in the first which has only moved with little other change. When found, this information is transmitted as a "motion vector" which takes a lot fewer bits for transmission than all of the original video frame. ('788 2:33-36.)

28. Decoding video information requires performing the inverse of these steps on incoming compressed data. For example, when video information is encoded as a motion vector, the decoding steps require accessing the specified block in the previous frame of video and determining its location in the current frame of video. Thus, enough decoded video data from the previous frame of video needs to be stored for this purpose. The '788 patent discloses holding the previous frame in the DRAM. For example, in a talking head video conference as

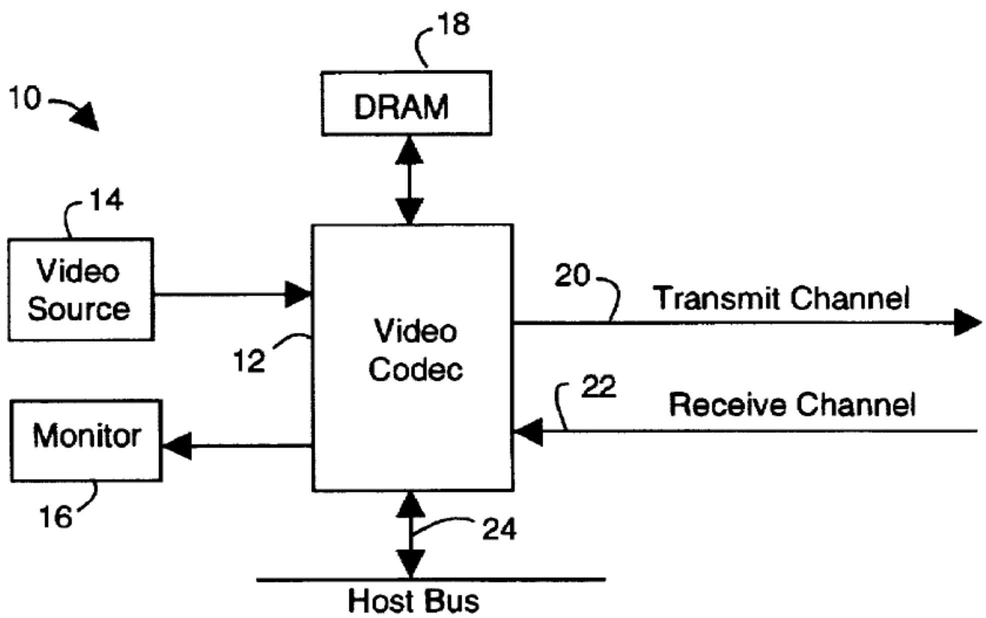
referenced at 1:36-39, there would be little movement of the persons head. Typically, under those conditions, much of video can coded as motion vectors, i.e., small variants on the previous. Therefore, as part of the decoding process, upon the receiving a motion vector, reference need only be made to the previous frame to work out what elements of the frame be reused entirely as is or by moving them by a specified number of pixels, up or down or left or right. This process within the community is sometimes referred to as "interframe decompression." The portion of the DRAM used to hold the previous is called a decoding frame buffer in the '788 patent (see '788 8:47). The decoding frame buffer must hold enough data to reconstruct the next frame being decoded, typically that is as complete decompressed frame.

29. The '788 patent describes holding enough video data of an uncompressed or decompressed frame of video data in the DRAM 18 for use during compression or decompression. For example, the '788 at 2:20-24 states that "[i]t is a still further object of the present invention to provide a single-chip video codec with a dynamic random access memory (DRAM) on-chip controller and interface that allows use of low cost memory system of external DRAMs." This passage conveys to me an architectural feature whose use recurs throughout the patent.

30. In describing Figure 1 at 3:43-45, the patent states that "[a] separate dynamic random access memory (DRAM) 18 provides storage for incoming and outgoing video data." In considering this sentence with reference to Figure 1, it conveys that incoming video data may be either compressed or uncompressed data depending on whether it is coming from the receive channel or video source, respectively. This figure also tells me that outgoing video data maybe compressed or decompressed data depending on whether it is output to the transmit channel or the monitor, respectively. This is so because Figure 1 shows two arrows bringing incoming

video data to the chip and two arrows carrying video data away from the chip:

Fig. 1



The importance of the sentence at 3:43-45 is that all four types of incoming and outgoing video data is streaming data and thus can only be temporarily stored in any DRAM of finite capacity.

31. Further, at 3:45-51, the patent states "Video information from the camera 14 or other video input source is compressed by the video codec 12 and transmitted out in compressed form on a transmit channel 20. Conversely, compressed video information is input to the video codec 12 from a receive channel 22, decompressed and output to the monitor 16 or other video output device, e.g., a television set." It is specifically noteworthy that the combination of 3:43-45 and 3:45-51 conveys that decompressed information flows from the DRAM to the monitor or other video device. At the time of the invention, the term "monitor" was typically used to refer to computer monitors, which usually accepted a VGA formatted input. The VGA format is different than PAL or NTSC format. The patent language in 3:50 refers to "a television set" as

being an example of another video output device. At the time of the invention a television set accepted PAL or NTSC formats. Thus, the patent is not restricted to outputting video data only in NTSC or PAL video data formats.

32. At 4:36, the '788 patent states: "As to be expected, decoding is the opposite of encoding." This point should be kept in mind when reading the patent. For example, the encoding process goes from serial video data to standard compliant video data and the decoding process starts with standard compliant video and produces serial video data for a monitor or other output device. Indeed, in some cases, the process for decoding is the inverse of the process for encoding. As I read this patent, there are many places where the process for decoding involves inverting the steps of encoding. In other places, such as those for example involving motion estimation, the process of decoding is simpler than the process of encoding. Further, standards bodies do not typically completely specify the codec.

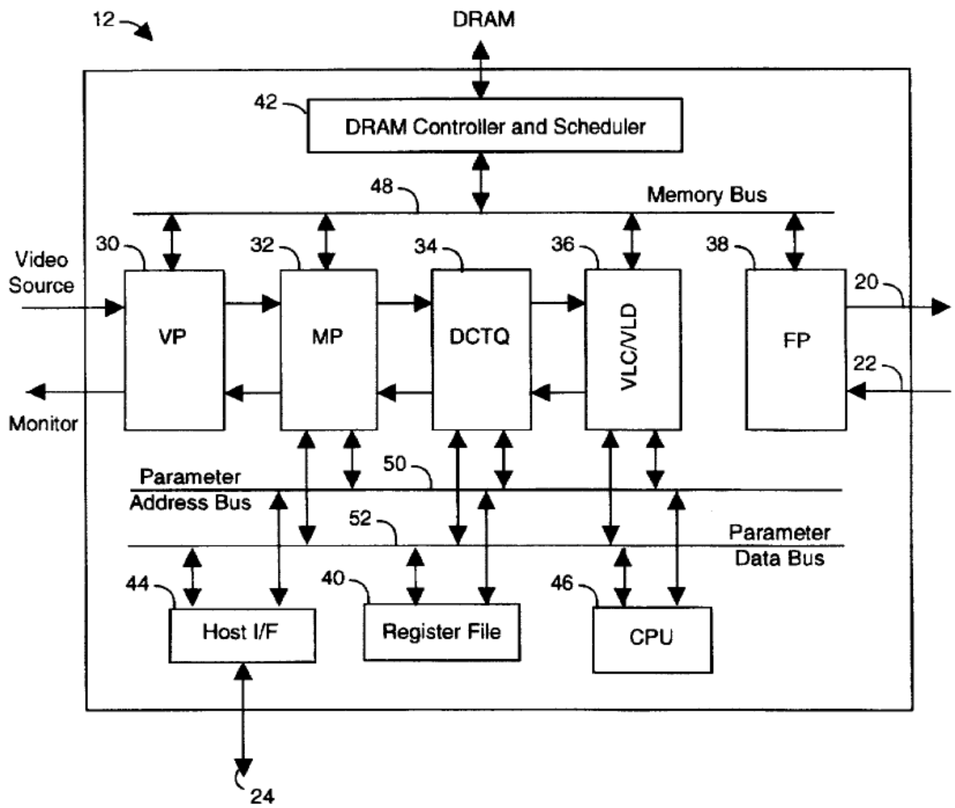
33. At 4:42-45 the patent states: "Within a macroblock, if it is type-intra, it is decoded using inverse zigzag, inverse quantizer and inverse discrete cosine transform and is sent out and stored in the frame memory in DRAM 18." This sentence tells me that the encoded video data (that the "macroblock") are decoded and stored in the frame memory in DRAM 18. At this point, the data that is stored in the frame memory is suitable for streaming to a monitor or other video output device.

34. In the same paragraph at 4:45-55, the patent states: "If it is type-inter, the decoded motion vector is used to motion-compensate the macroblock in a previous frame 't-1'. At the same time, the differences between "t" and "t-1" are decoded using inverse quantizer, zigzag and discrete cosine transform. These decoded differences, are added to a motion-compensated macroblock, to reconstruct macroblock for the current frame 't'. The re-constructed macroblock

is the output of the decoder and is stored in the frame memory in DRAM 18 for reconstructing the next frame 't+1'." This passage and 4:42-45 describe the process of building the current frame "t" for storage in the DRAM from a preceding frame "t-1" or solely from the incoming encoded video stream. Inter-frame decoding uses the motion vector to produce the macroblock in frame "t" from the macroblocks in frame 't-1." This passage is another place establishing that decoded video is being stored in the DRAM frame memory. Thus, macroblocks produced from both intra- and inter- decoding processes are retained in case they are needed in the next t+1 frame. In addition, as the passage teaches that the data is stored in a "frame memory in DRAM 18," it tells me that as much as one complete reconstructed frame of video data may need to be stored in the DRAM 18. Further, at this point the data is suitable for streaming to a monitor or other video output device.

35. At 4:63-65 of the patent, in discussing Figure 2, it is stated that "The video input/output buffer (VP) 30 is such that the incoming pixels are buffered and stored in the external DRAM 18 for raster-scan-to-block conversion." Raster-scan-to-block is a term of art that describes two different data formats; in the raster-scan format the data is arranged as a sequence of rows of pixels, and in the other format the data is arranged as macroblocks of pixels. As used in 4:63-65, this term of art is referring to a difference between the line format of the data used by cameras or video sources and monitors or video output devices, and the macroblocks of data used by the chip in the encoder and decoder. As shown in Figure 2, incoming pixels arrive at the VP 30 from both the video source and the MP 32 block. As also shown in Figure 2, there is also a two way connection between VP30 and the DRAM 18 via memory bus 48; there is also a two way connection between the MP 32 and the VP 30:

Fig. 2



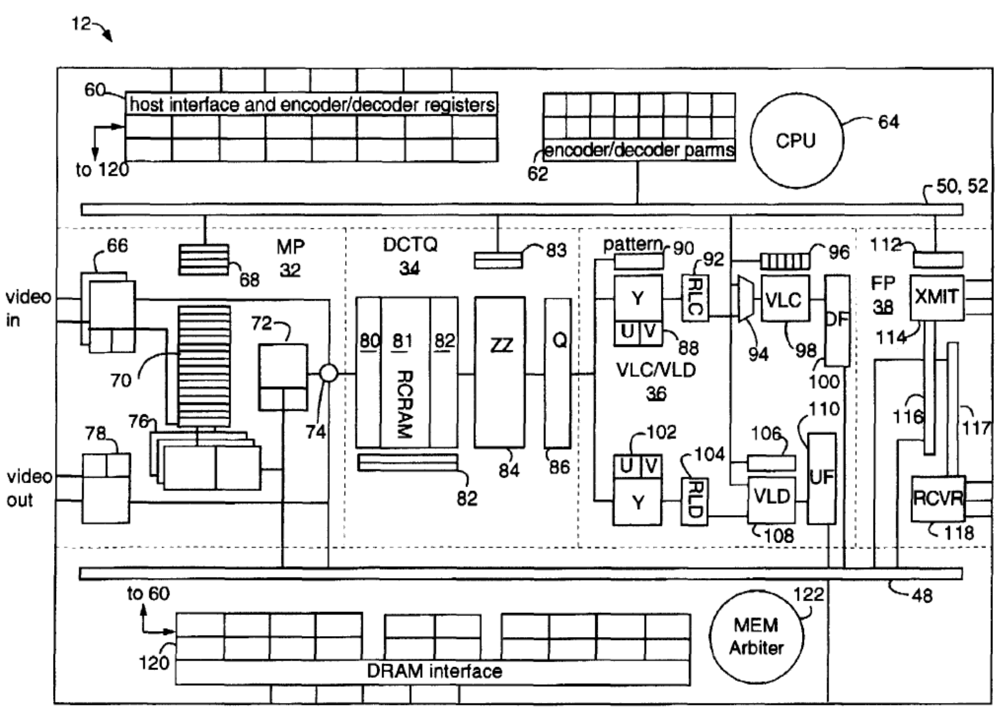
The two way connection between the DRAM memory bus 48 and video buffer tells me that data from the DRAM is provided to the video output buffer (VP 30). The two way connection between VP 30 and MP32 tells me that data is passing between MP32 and VP30. Further, there is an arrow out the chip from VP 30, which tells me that data from VP 30 is transmitted out from the chip.

36. At 5:29-34, the patent states: "The DRAM controller 42 manages access to the *frame buffer* and the transmit/receive buffer. It schedules memory cycles for the encoder and decoder. In addition, users can set the sizes of *encoding and decoding frame buffers*, as well as the transmit and receive buffers." As stated, the DRAM controller 42 manages all four buffers for the chip. The reference here to "frame buffer" is to the locations in the DRAM 18 for storing

uncompressed and decompressed video frames as previously discussed above. It also indicates that there are two additional transmit and receive buffers. The DRAM controller schedules access to these four buffers. In addition, this sentence allows for resizing of the buffers as needed or desired. In particular, the storage space of the encoding and decoding frame buffers can be varied to hold different amounts of uncompressed and decompressed video data, including for example one or more frames. Resizing the buffer may also be appropriate when changing the video format, for example between CIF and QCIF which are discussed in the patent.

37. "FIG. 3 shows the video codec 12 in more detail than FIG. 2." ('788 5:46-47; which is also stated at 3:16-17.) This indicates that Figures 2 and 3 are related. Although Figure 3 provides more detail on Figure 2, this sentence indicates that these drawings complement each other. Figure 3 shows the macroblocks input and output to and from the MP 32:

Fig. 3



As shown on Figure 2, MP 32 has a two way connection to VP 30. Thus, it necessarily follows that the "video in" and "video out" on Figure 3 interfaces with the VP 30 on Figure 2. In particular, other parts of the patent indicate that the MP32 writes reconstructed macroblocks to the DRAM (*see*, *e.g.*, 4:52-54 and 11:24-35).

38. At 5:66-67 the patent states: "A video output, e.g., to the monitor 16, is provided from a reconstructed macroblock 78." In this sentence "from a reconstructed macroblock" tells me part of a macroblock is buffered in block 78 of Figure 3 and is used to provide output to the monitor. Since 3:43-45 states that outgoing video data is stored in the DRAM, then the buffer in block 78 is buffering data from the DRAM and, as shown in Figure 3, is connected to the DRAM through DRAM bus 48. It should be noted that block 78 is the video out of MP 32 of Figures 2 and 3 ("FIG. 3 is a more detailed block diagram of the single-chip video codec of FIG. 2"). As such, the video out in Figure 3 comes from a reconstructed macroblock that is input to the VP 30 in Figure 2. Therefore, a video output to, for example, a monitor may be provided from reconstructed macroblocks that enter VP30. These macroblocks are also necessarily stored in the DRAM 18 as described above. My understanding of the '788 patent is that the reconstructed macroblocks that are held in the DRAM are the same macroblocks that are necessarily output from the chip to a video output device.

39. At 6:10-13 the patent states: "When decoding, the motion predictor 32 reconstructs each video frame by adding a received-frame difference to a frame prediction based on previous reconstructed frames." As previously discussed, this sentence reiterates the point that the decoder may require a fully decoded ("reconstructed") frame to be held in memory in order to decode the subsequent frame.

40. At 8:43-57 the patent states: "Local memory and the DRAM controller 42 provide

data transfer supports to the pipelined video codec operations on a macroblock cycle basis. The DRAM 18 is partitioned by the video codec 12 into four sections, (1) an encoder frame buffer (EFB), (2) a decoder frame buffer (DFB), (3) a transmission channel buffer (TCB), and (4) a reception channel buffer (RCB). The section start address and the section size in words or double-words are programmable, and the section start addresses must be at word and double-word boundaries respectively. All of the memory sections operate in a wrap-around fashion, wherein the read/write pointer automatically jumps back to the starting address after hitting the section's ending boundary. The order of data storage in each section is sequentially consistent with the H.261 standard and thus DRAM 18 is preferably a page-mode type to allow faster memory accesses." This disclosure identifies and describes the DRAM controller 42 operations to support cyclic movement of data to and from the DRAM 18 for each of the four input/output (I/O) ports of the chip. Of interest here is the decoder frame buffer (DFB) which would contain the one or more decompressed (reconstructed) frames which have been previously described. As described in this section of the patent, the macroblocks are stored in a wrap-around fashion so that the macroblocks can be stored in an orderly way that benefits from the DRAM's page mode memory access. In addition, the reference to a "wrap-around" operation means that all the data in the DFB (and other buffers) is periodically overwritten, emphasizing the temporary nature of the store. In addition, the "wrap-around" operation applies to read operations indicating that it is used for outputting video data from the chip. This passage also points out that decoder buffer is a frame buffer in reference to a frame of video data.

41. At 11:24-35, the patent states: "The decoder write {dw} is an access that stores one whole macroblock sequentially from the reconstruction adder into the decoder frame buffer. In pseudocode,

Initialize at programming DWA = decoder frame buffer starting address

{dfa};

At DWRQ do {

issue DWAK;

repeat (96) { store IMD 31:0! into mem DWA!; DWA++ };

}"

This tells me that the macroblocks are written one complete macroblock at a time to the decoder frame buffer (DFB) in the DRAM. If each pixel of data takes 12 bits, then one macroblock of data is 96 words long (as the patent indicates that the IMD is a 32-bits long word). Further, the pseudo-code includes the words "repeat (96)." The words in the pseudo-code "DWA++" refers to a common computer language construct implying sequential addressing. In addition, the phrase reconstruction adder refers to the adder/subtracter 74 (see 6:45). This pseudo-code teaches how to sequence reading of the memory to read out pixels in a raster-scan fashion. For example to read out the first row of pixels, I would first read out words 0-6 of this part of the memory and then words 96-101, representing the required portions of the first two macroblocks. This is yet another passage that indicates that reconstructed macroblocks are being stored in the DFB of the DRAM 18 and, when considered with the other disclosures discussed above convey that the reconstructed macroblocks are used to provide output to the video output connection. And furthermore at 11:42-50, the patent gives an example of reading data from memory.

42. At 14:36-38, the patent states: "A mixer 414 produces a decoded output which is copied to a frame memory 416, e.g., in DRAM 48." As shown in Figure 7, the encoded data is fully decoded and then stored in the frame memory, which is identified in Figure 7 as block 416, and in Figure 1 as the DRAM 18. Notably, Figure 7 is a "prior flow diagram representing the functional connections of the 'H.261' standard decoding process which is implemented by the video codec (FIG. 2) while in decoder mode." (14:29-32.)

43. Altogether, the units described in the '788 patent (1) decompress the encoded video information arriving from the receive channel 22, (2) stores the decompressed video as complete frames to the DRAM, (3) reads out the decompressed video from the DRAM in a piecemeal fashion to the video output connection, (4) uses the complete stored decompressed frame to assist in the decompression of the next frame, and, once the next frame is decompressed, (5) the decompressed frame is eventually overwritten so that it is no longer stored in the DRAM. Each of steps (1)-(5) are described above in greater detail. Specifically, step (1) is described in paragraphs 22, 24, 28, 29, 30, 31, 32, 33,and 34; step (2) is described in paragraphs 21, 28, 29, 30, 33, 34, 36, 40, 41, and 42; step (3) is described in paragraphs 31, 36, 38 and 41; step (4) is described in paragraph 34; and step (5) is described in paragraph 40.

44. "[S]torage of . . . outgoing video data," as it appears at 3:43-52 of the '788 patent, conveys that compressed video data is stored in DRAM 18 and output on channel 22 and, conversely, that decompressed video data is stored in DRAM 18 and output to a monitor 16. Thus, more than one type of outgoing video data is stored in the DRAM. Further, since 8:45-49 tells me that the DRAM has a decoder frame buffer (DFB) and a transmission channel buffer (TCB), these buffers are used in the DRAM to store outgoing video data. The outgoing video data that is stored in the DFB is in the form of decompressed video data that is ready for output to a monitor, or other video output device.

45. Further, as indicated paragraphs 30 and 40 above, DRAM memory is finite in nature and video information being extremely large in nature means that the DRAM as described in the '788 patent temporarily stores data. In addition, given that the DRAM is described as being operated in "wrap-around fashion" the DRAM necessarily stores data temporarily.

46. As indicated above, the DRAM is used to hold at least one fully decompressed

frame of data that is ready for output. That is, interim storage in the DRAM of video data that is decompressed prior to is passing through the video output connection is supported by the '788 patent. In paragraphs 33, 34, 40, 41 and 42, I have discussed how the specification of the '788 patent discloses interim storage of decompressed data in the DRAM prior to its passing through the video output connection to the DRAM. Therefore, the specification reasonably conveys to me, as it would to one skilled in the art, that there is interim storage of outgoing video data in the DRAM, as well as interim storage of decompressed data in the DRAM prior to its passing through the video output connection to the DRAM. Accordingly, I disagree with the statements contained in Defendants' papers at page 11 that states: "there is no support for interim storage in the DRAM of decompressed video data prior to its passing through the video output connection."

47. As indicated above in paragraphs 30, 31 and 43 above, I disagree with the Defendants' characterization of 3:43-51 of the '788 patent as they have stated in their brief at page 12. This passages makes clear that the DRAM is used for storing incoming and outgoing video data and that incoming and outgoing video data includes compressed, uncompressed and decompressed video data. This passage further states that the outgoing video data is decompressed video data that may be output to a monitor or other video output device.

48. Defendants also mischaracterize AVT's reliance on Figure 3 in their brief. (Defs. brief at 13.) As indicated in paragraphs 37, 38, 39 and 40, I disagree with Defendants that Figure 3 provides no written description of interim storage of outgoing video data. When considering Figures 2 and 3 together as I do above in paragraph 38, data from macroblocks 78 are output to the VP 30. Further, these reconstructed macroblocks stored in DRAM 18 and are used to provide a video output to, for example, a monitor or output video device. In this regard, the patent reasonably conveys to me that the reconstructed macroblocks that are held in the DRAM

are the macroblocks that are used necessarily output from the chip to a video output device. It should be clear to one skilled in the art that a frame memory contains all the macroblocks in one frame of video and that showing the movement of macroblocks, as in Figures 2 and 3, describes the movement of video data that is required to produce a frame. Also, as described in paragraph 36 above, a full previous frame must be stored in order to decode the next frame, and the DRAM frame memory is used to hold this frame. Therefore, Figure 3 is illustrative when taken in context with Figure 2 and I as I describe in paragraphs 37 – 41 above, and shows that decompressed video data is temporarily stored in the DRAM prior to being output to a video output device. In summary, reconstructed frames of video are temporarily stored in DRAM and are ultimately output to a video device from the DRAM.

49. I also disagree with Defendants statement on page 15 of their brief that 4:52-55 ("The re-constructed macroblock is the output of the decoder and is stored in the frame memory in DRAM 18 for reconstructing the next frame "t+l".) and 5:66-67 ("A video output. e.g.. to the monitor 16, is provided from a reconstructed macroblock 78.") of the patent, because they may appear one column apart, are unrelated to each other. This is incorrect for a number of reasons. First, this is a single patent and the concept of a macroblock is discussed consistently throughout the patent *e.g.,* Cols 4 and 5. Second, at 4:52-55 the patent states that "the reconstructed macroblock is the output of the decoder and is stored in the frame memory in DRAM 18 for reconstructing the next frame 't+1'." As explained above, as part of the decoding process, the patent describes that a decoded frame made up of reconstructed macroblocks needs to be stored to decode the macroblocks in frame t+1. The reconstructed macroblocks that makeup the decoded frame is the video data that is outgoing through the video buffer from the DRAM. Although a minimum number of reconstructed macroblocks need to be stored in the DRAM 18

before they can be read out from the memory through VP 30 to a monitor, there is no question that the reconstructed macroblocks are output to a monitor as is clearly stated at 5:66-67. Thus, reconstructed macroblock as described at 4:52 and 5:66-67 are one in the same and the patent explicitly teaches at 5:66-67 that it these macroblocks that are output to for example a monitor.

50. I also do not agree with the second bullet point in page 16 of defendants' brief. That bullet implies that the decoder frame buffer only stores data during decompression by the codec. The decoder frame buffer certainly stores a fully decompressed frame of data as discussed in paragraphs 36 above. However, the decoder frame buffer may also be used to store partially decoded data.

51. As indicated above in paragraph 41, the decoder write psuedocode discloses how reconstructed macroblocks are written to the DRAM and thus how they can be read from the DRAM in raster-scan fashion. Thus, I disagree with defendants' statement that "there is no instruction in the code to fetch from, or store on, the DRAM fully decompressed video data." (Pg. 16, n.1)

52. I disagree with defendants statement No. 5 in the Statement of Undisputed Facts ("SUF") that the "codec chip digitizes analog signals from a video source." As indicated at 4:63-65 of the '788 patent, the "video input/output buffer (VP) 30 is such that the incoming pixels are buffered." Pixels are "picture elements" and are a digital representation of that picture element (see 1:22-25). I agree with defendants statement in SUF No. 5 that digitized video information consists of a series of frames, each frame having close to one million pixels as indicated at 1:27-28 of the '788 patent.

53. The level of detail of the specification, *e.g.*, pseudo-code in columns 9-12, clock frequencies in 2:6-7, calculations in 6:18-51, etc., indicates to me that the inventors worked out

many engineering details of the internal operations of the chip and its external interfaces.

I declare under penalty of perjury that to the best of my knowledge, information and belief, the foregoing statements are true and correct.

Dated: May 10, 2013

Signed: Paul D Franzon

Dr. Paul D. Franzon